AMENDMENTS TO THE CLAIMS:

Please cancel claims 4 and 9, without prejudice. Kindly amend claims 1-3 and 5- 8, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (currently amended): A delay producing method [[using]] which uses first-stage to ~~N[th]-stage~~ N^{th} stage delay elements connected in series to each other and which, when a clock signal is inputted to ~~an input side~~ a first delay stage node of said first-stage delay element, ~~producing an even-stage delayed signal from a clock signal obtained from the even-stage delay element, and an odd-stage delayed signal from a clock signal obtained from the odd-stage delay element,~~ said delay producing method produces the clock signal through the first delay stage node and delayed signals outputted through second to $(N+1)^{th}$ delay stage nodes of the second through the N^{th} delay elements, respectively, said delay producing method for producing an even clock signal and an odd clock signal comprising:

using a first-stage selector and second-stage to ~~N[th]-stage~~ $(N+1)^{th}$ stage selectors arranged in one-to-one correspondence with ~~said delay elements~~ said first delay stage node to $(N+1)^{th}$ delay stage nodes, and each of the first through the $(N+1)^{th}$ stage selectors outputting one selected from two inputs;

using, as one of inputs given to each of said first-stage selector to ~~N[th]-stage~~ $(N+1)^{th}$ stage selector[[s]], an input given to a corresponding one of said ~~delay elements;~~ first delay stage node to the $(N+1)^{th}$ delay stage nodes;

using, as the other of [[the]] inputs given to each of said first-stage selector and the second-stage to $(N+1)^{th}$ ~~to (N-1)[th]~~ stage selectors, an output from $(n+2)^{th}$ one of the third

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through (N+1) stage selectors, where n is a variable between 1 and (N-1); outputting said even clock signal from said first-stage selector; and ~~said selector of the next but one stage;~~ outputting said odd clock signal from said second-stage selector.

~~outputting said even-stage delayed signal from said first-stage selector; and~~

~~outputting said odd-stage delayed signal from said second-stage selector.~~

Claim 2 (currently amended): . The delay producing method according to claim 1, wherein delay amounts of said first-stage to ~~Nth-stage~~ Nth stage delay elements are equal to each other.

Claim 3 (currently amended): The delay producing method according to claim 1, wherein said first-stage to ~~Nth-stage~~ Nth stage delay elements ~~have different delay amounts~~ are divided into a first group of the first through m-th stage delay elements and a second group of the (m+1)-th through N-th stage delay elements, where m is an integer smaller than N;

the first group of the first through m-th stage delay elements having delay amounts different from the second group of the (m+1)-th through N-th stage delay elements.

Claim 4 (canceled)

Claim 5 (currently amended): A delay producing circuit including first-stage to ~~Nth-stage~~ Nth stage delay elements connected in series to each other and, when a clock signal is ~~inputted to an input side of said first-stage delay element,~~ input to a first delay stage node of said first-stage delay element, producing the clock signal through the first delay stage node and delayed signals outputted through second to (N+1)th delay stage nodes of the second through the Nth delay elements, respectively, the delay producing circuit being for producing an even clock signal and an odd clock signal and ~~producing an even-stage delayed signal from a clock signal obtained from the even-stage delay element, and an odd-stage delayed signal from a clock signal obtained from the odd-stage delay element, said delay producing circuit~~ comprising:

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a first-stage selector and second-stage to ~~N^th^-stage~~ (N+1)^th^ stage selectors arranged in one-to-one correspondence with said first delay stage node to (N+1)^th^ delay stage nodes, and each of the first through the (N+1)^th^ stage selectors ~~elements, and each~~ having two input terminals and one output terminal[[,]];

wherein one of the input terminals of ~~each of said~~ the first-stage ~~to N^th^-stage selectors~~ selector is connected to ~~an input side of a corresponding one of said~~ the first delay stage node of the first-stage delay element while one of the input terminals of the second-stage through (N+1)^th^ stage selectors is connected to the second through (N+1)^th^ delay stage nodes, respectively; ~~elements, the other of the input terminals of each of said first-stage to (N-1)^th^-stage selectors is connected to the output terminal of said selector of the next but one stage, said even-stage delayed signal is outputted from the output terminal of said first-stage selector, and said odd-stage delayed signal is outputted from the output terminal of said second-stage selector.~~

wherein the other of the input terminals of the first through the (N+1)^th^ stage selectors is connected to the output terminal of (n+2)^th^ one of the third through the (N+1)^th^ stage selectors, where n is a variable between 1 and (N-1);

wherein the first-stage selector produces the even clock signal through the one output terminal of the first-stage selector while the second-stage selector produces the odd clock signal through the one output terminal of the second-stage selector.

Claim 6 (currently amended): The delay producing circuit according to claim 5, wherein delay amounts of said first-stage to ~~N^th^-stage~~ N^th^ stage delay elements are equal to each other.

Claim 7 (currently amended): The delay producing circuit according to claim 5, wherein said first-stage to ~~N^th^-stage~~ N^th^ stage delay elements ~~have different delay amounts~~ are divided

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into a first group of the first through m-th stage delay elements and a second group of the $(m+1)^{th}$ through N^{th} stage delay elements, where m is an integer smaller than N:

the first group of the first through m^{th} stage delay elements having delay amounts different from the second group of the $(m+1)^{th}$ through N^{th} stage delay elements.

Claim 8 (currently amended): [[A]] The delay ~~adjusting circuit using said delay~~ producing circuit according to claim 5, further comprising a delay fine adjusting circuit that synthesizes ~~said even-stage delayed~~ the even clock signal and ~~said odd-stage delayed~~ the odd clock signal with each other and applies a fine adjustment thereto to ~~thereby~~ produce and output an internal clock signal.

Claim 9 (canceled)

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